IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-11 (Canceled).

Claim 12 (Currently Amended): A decoding apparatus configured to decode compression-encoded video data including a variable length code, comprising:

a plurality of decompression ~~devices configured~~ processors to decompress a plurality of compression-encoded video data corresponding to a plurality of channels, respectively, each of the decompression ~~devices~~ processors including:

a variable length decoder which decodes the variable length code to output [[a]] zero-run length data and [[a]] nonzero coefficients;

an inverse quantizer which inverse-quantizes the nonzero coefficients to output an inverse-quantized result;

a zero-run reconstruction ~~processor which~~ device configured to reconstruct zero coefficients corresponding to the zero-run length data; and

a FIFO (First-In First-Out) memory arranged between the inverse quantizer and the zero-run reconstruction ~~processor~~ device, ~~and~~ configured to store the ~~zero-run length data and~~ nonzero coefficients of the inverse-quantized result, the memory operating with first-in first-out and having a memory capacity for storing coefficients contained in a plurality of blocks;

a plurality of parameter extractors provided corresponding to the decompression ~~devices~~ processors, ~~and~~ configured to generate parameters concerning one macro-block every time the variable length decoder included in each of the decompression ~~devices~~ processors completes decoding of one block; ~~and~~

an inverse discrete cosine transformer which subjects the coefficients from the decompression ~~devices~~ processors to inverse discrete cosine transformation to obtain transformed coefficients; and

a motion compensator which subjects the transformed coefficients to a motion compensation in accordance with the parameters concerning one block input from the parameter extractors alternately.

Claim 13 (Original): An apparatus according to claim 12, wherein the variable length decoder decodes the variable length code corresponding to a macro block including a predetermined number of blocks.

Claim 14 (Currently Amended): An apparatus according to claim 12, wherein the zero-run reconstruction ~~processor~~ device includes a buffer memory configured to write in the zero coefficients and the nonzero coefficients therein at a write-in speed and read out them therefrom at a readout speed higher than the write-in speed.

Claim 15 (Currently Amended): An apparatus according to claim 12, wherein if the nonzero coefficients ~~does not~~ fail to exist at a final position of a block when the inverse quantizer receives a block end signal indicating the end of the block from the variable length decoder, the inverse quantizer generates a zero coefficient as ~~the~~ a final DCT coefficient of the block.

Claim 16 (Currently Amended): An apparatus according to claim 12, wherein the variable length decoder stops its output in units of one coefficient when the inverse quantizer

~~is unreceivable~~ fails to receive the zero-run length data and the nonzero coefficients from the variable length decoder.

Claim 17 (Currently Amended): An apparatus according to claim 12, wherein every time the inverse quantizer receives the zero-run length data from the variable length decoder, the inverse quantizer accumulates a value obtained by adding "1" to the zero-run length data and generates scan address data indicating a coefficient position of the nonzero coefficients, to generate quantization step size data for every coefficient position based on the scan address data and scan pattern data indicating ~~the~~ a scan pattern.

Claim 18 (Currently Amended): An apparatus according to claim 12, wherein the zero-run reconstruction ~~processor~~ device includes an internal scan address counter increased one by one for each clock, and rejects next data input from the FIFO memory until a scan address received from the FIFO memory has coincided with a count value of the internal scan address counter, to generate the zero coefficients corresponding to the zero-run length data.

Claim 19 (Original): An apparatus according to claim 12, which includes an intra-dc reconstruction device configured to reproduce dc components contained in the coefficients in intra-blocks in parallel with inverse quantization of the inverse quantizer.